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Effects of gate shaping and consequent process changes on AlGaIn/GaN HEMT reliability

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The effect of gate shape and its necessary fabrication process on the reliability of AlGaIn/GaN high electron mobility transistors (HEMT) was studied on devices fabricated on the same wafer, using DC and pulsed HEMT analysis. Simulations were used to determine the difference in electric field on the surface and in the barrier for the three gate shapes studied, I-shaped, slanted and recessed slanted. Prior to each electrical characterization during stress, devices were exposed to ultraviolet illumination to probe only newly generated traps rather than the filling of pre-existing electronic traps. Degradation was seen to increase with electric

field strength; in each device type traps were generated by device stress at the location of the peak electric field. It was found that HEMTs with I-shaped gates showed larger degradation under the same stress conditions than devices with slanted gates. This was due to a higher electric field at the interface between the SiN_x passivation and the AlGaIn barrier layer resulting in higher surface trap generation. HEMTs with slanted recessed gates showed indications of barrier trapping while surface trapping effects played a smaller role.

1 Introduction

AlGaIn/GaN high electron mobility transistors (HEMTs) have attracted great attention in the semiconductor community due to their excellent RF power performance and robustness [1, 2]. They are the subject of reliability research in order to determine the mechanisms that drive their degradation, as at present reliability issues are still a concern. Electronic trap generation has been found to be an important limiting factor for device reliability [3]. However, detailed mechanisms behind many degradation issues of AlGaIn/GaN HEMTs are not yet fully established, with reliability improvement methodologies currently being largely empirical. The occurrence of traps (both pre-existing and stress induced) has been studied with different techniques including optical as well as electrical techniques; traps with activation energies of 0.12 eV and 0.45 eV as well as 0.5 eV have been found, predominantly located in the drain access region next to the gate contact [4, 5]. Usual degradation effects include, in varying combina-

tions, a change in maximum drain current, gate leakage current increase, changes of the transconductance characteristic, a shift in the threshold voltage as well as an increase in drain current dispersion [6]. A number of device structure modifications have been proposed to suppress these effects and consequently improve the devices' reliability including surface passivation which succeeded in minimizing gate leakage currents and electron trapping effects [7,8] while others employed different cap layers between the gate contact and the passivation layer [9]. Field plates have been used to spread and smooth electric field distributions (which are typically in the MV/cm range) at junctions to increase the breakdown voltage [1]. In particular, different gate shapes were used to reduce peak electric fields and to mitigate device degradation [10]. It has been observed that defect generation at either the semiconductor top surface or in the AlGaIn layer of a device can be responsible for device degradation [11], including potential contributions from oxygen related defects [12, 13] and dis-

locations [14]. In a more pronounced degradation stage surface pitting has also been observed [15]. Stressing at pinch off conditions showed an increase in gate leakage currents and the creation of defects through mechanisms that are not fully understood [16]. In this work AlGaIn/GaN HEMTs fabricated on the same wafer, but with different gate shapes were investigated to gain insight into the effect of the gate shape on trap generation in the device. This approach eliminates any effect on the study of material and process variations other than those needed to generate the different gate shapes. Devices with a slanted gate, with or without gate recess, are compared with a simple I-shaped gate as a reference.

2 Experimental Details

AlGaIn/GaN HEMT devices studied here were grown by metal organic chemical vapor deposition (MOCVD) on a SiC substrate with a 2 μm semi-insulating GaN buffer, 0.7 nm AlN interlayer and 25 nm thick AlGaIn barrier layer (26% Al content). The HEMTs had standard Ohmic source and drain contacts with a gate-source spacing of 0.5 μm and a gate-drain spacing varying between 2 and 6 μm for all gate shapes. Three gate shapes were considered, all fabricated on the same wafer: I-shaped, slanted and slanted recessed as illustrated in Figure 1 with a gate width of 150 μm . The 0.9 μm long I-shaped gate was deposited first followed by the deposition of the 160 nm SiN_x passivation layer. In the case of the other two gate shapes, the passivation layer was deposited first and 55° slanted sidewall openings etched into it using a CF₄/O₂ reactive ion etch. For the recessed device 15 nm of the AlGaIn barrier was removed using a Cl₂ plasma etch followed by a 15 s CF₄ etch to reduce gate leakage.

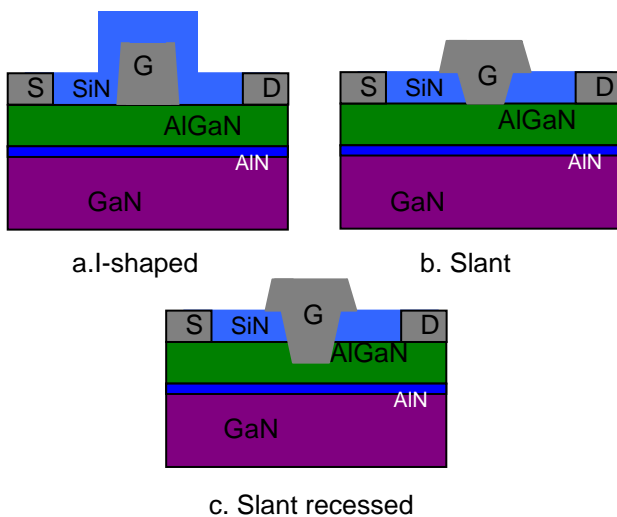


Figure 1 Schematic of the studied AlGaIn/GaN HEMTs with different gate shapes, (a) I-shaped, (b) slant and (c) slant recessed gates (not to scale).

This was followed by the deposition of the slant gate metal, which also formed an integrated gate connected field plate of 0.25 μm length. The results discussed here correspond to a 1 μm long slant gate and a 0.7 μm long slant recessed gate. Standard Ni/Au gate contact metallizations were used in all cases. Further details of the tested device structures can be found in reference [10].

All three device types were stressed under the same bias conditions: 20 hours of voltage bias stress in the off-state at a drain source voltage of 20 V at a gate voltage 0.5 V below the threshold voltage V_{th} ($V_{th} = -5\text{V}$ for both I-shaped and slant gate devices, $V_{th} = -2.5\text{V}$ for the slant recessed gate device). Measurements were performed on 3 devices each showing similar results; and in the following representative results are shown. During stress, drain and gate current were monitored with time while every 2 hours stress was interrupted for more extensive electrical testing, namely DC output characteristics, transconductance and threshold voltage, gate lag (the gate had 0.1 μs long pulses at open channel separated by 0.1 ms at pinch-off, while the drain was DC biased) as well as drain current (I_d) transient measurements. The latter was performed to measure the trap density by applying an off-state voltage pulse (-10V) at the gate contact for 1 s filling or emptying traps depending on their location in the device. The gate was then pulsed to 1V with a drain voltage of 0.5 V and the effect of de-trapping monitored via recording I_d and representing results in terms of $dI_d/d(\log(\text{time}))$ against $\log(\text{time})$, which allows discrimination of different trap levels. More details on the technique can be found in [4]. Prior to all of the electrical testing, i.e. before and after stress, at every 2 hour interval as well as after a control measurement after 8hrs of device inactivity, the devices were exposed to UV illumination at 344 nm for 30 s. This de-populated all pre-existing traps, so that only newly generated traps are measured in the electrical analysis. The technique can therefore distinguish between recoverable and permanent device degradation.

Figure 2 shows representative results of I_d transient measurements as part of an analysis that established 344 nm as the optimal wavelength to de-trap pre-existing electronic traps in the device. It also demonstrated the effectiveness of the UV illumination approach. Different peaks can be distinguished in Figure 2 showing the diversity in trap emission time, predominantly showing two trap types, denoted here Tp1 and Tp3, similar as in Ref[4]. Measurements were taken before and after stress as well as after 8 hours of device inactivity. In this experiment voltage stress was applied for 1 hour only so that pre-existing traps are filled, but no significant new trap generation occurred in the device. The two recovery methods under investigation here were UV illumination for 30 seconds (Figure 2a) as well as device inactivity for 8 hours (Figure 2b).

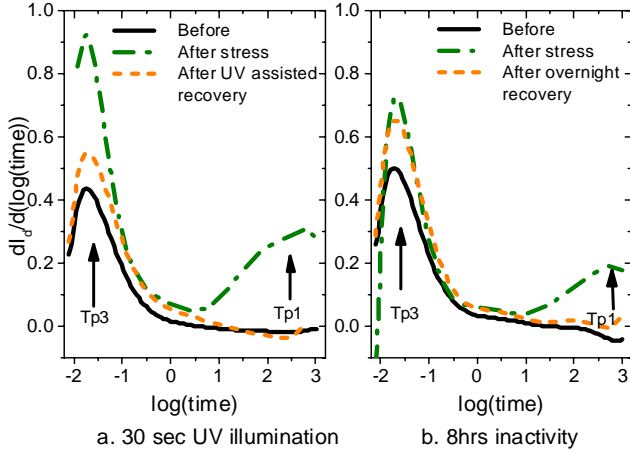


Figure 2 I_d transient trapping characteristics $dI_d/d(\log(\text{time}))$ as a function of time of AlGaIn/GaN HEMTs with I-shaped gate after 1 hour of off-state stress at $V_{ds}=20\text{V}$, $V_{gs}=V_{th}-0.5\text{V}$ and after 30 sec of UV illumination (a) and 8 hours of device inactivity (b).

The height of the trap peaks increases with stress and then decreases close to the initial levels following both recovery methods (UV illumination and 8 hour long device inactivity), i.e. insignificant numbers of traps are generated. This supports the use of UV illumination during the subsequent 20 hours stress analysis to eliminate signals of pre-existing traps from the measurements and to allow analysis of device degradation only. It removes the need for an 8 hour rest period which is not practical to perform in long-time reliability testing. Visible light illumination has been used in the past to measure electrical characteristics independent of trapping effects for different devices [17], while only broad band UV illumination in particular has been used during electrical stressing [18].

3 Results and Discussion

Figure 3 illustrates DC output characteristics of the AlGaIn/GaN HEMTs prior to and after electrical stress. Different features in the stress-induced changes are apparent for devices with different gate shapes. For HEMTs with an I-shaped gate, a change in slope in the linear region together with a reduction in the maximum drain current (I_{dmax}) can be observed. For HEMTs with a slant gate, a smaller decrease in slope in the linear region is apparent, and an increase in the maximum drain current I_{dmax} is found. The slant recessed gated device shows no change in slope, but an increase in I_{dmax} is found. The percentage change of the slope of the DC characteristics shown in Figure 3 is further emphasized in Figure 4. A decrease of the drain current I_d after stress can only be observed for I-shaped gated devices. In contrast the DC characteristics of slant gated devices, with and without recess, are dominated by a threshold voltage shift. This is represented by an increased I_{dmax} and is further confirmed by extrapolated V_{th} values from transconductance measurements as seen in Figure 5b.

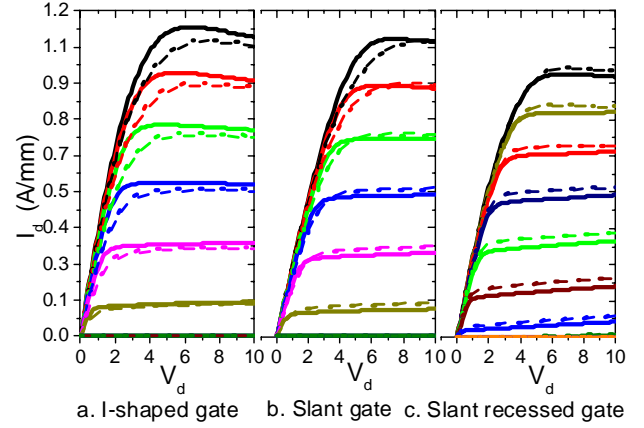


Figure 3 Output characteristics of AlGaIn/GaN HEMTs for (a) I-shaped, (b) slant and (c) slant recessed gates prior to stress (solid line) and after 20 hrs of off-state stress at $V_{ds}=20\text{V}$ (dashed line). Measurements after a subsequent 8 hrs of device inactivity showed no further change or evidence of recovery. V_{gs} values were stepped from 1V to -6V in steps of 1V for the I-shaped and slant gates devices, while for slant recessed gated devices V_{gs} was stepped from 1V to -3.5V in 0.5V steps.

We will now discuss how this data shows that traps are generated by stress in different locations for different gate shapes. A change in slope in the linear region indicates a change in the source (R_s) or drain (R_d) resistance, while an increase in R_s (but not R_d) also causes a decrease in maximum drain current I_{dmax} . The decrease in I_{dmax} and slope with the resultant shift in knee voltage, which is observed for the I-shaped gated device in Figure 3a, suggests trap generation on the AlGaIn surface resulting in a virtual gate effect [19]. As the device was exposed to UV illumination prior to measurements these are traps newly generated by stressing.

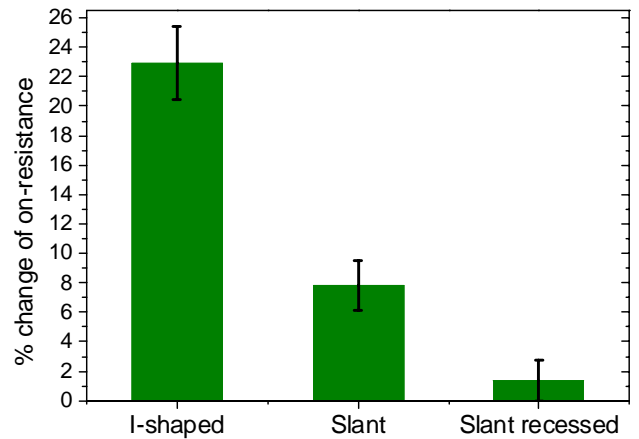


Figure 4 Percentage change of the on-resistance due to 20 hours of electrical stress for I-shaped, slant and slant recessed gated devices. Values extrapolated from data corresponding to Figure 3.

A different form of degradation following stress is observed for either the slant gated or slant recessed gated devices. The slanted non-recessed device shows a much smaller decrease in the linear slope, i.e. a change in linear resistance and much smaller knee-walkout, indicating a smaller contribution from surface traps. However, for slant non-recessed gated devices there is in addition a consistent increase of I_{dmax} for all V_{gs} values indicating a threshold voltage shift due to stress-induced barrier traps underneath the gate. For the slanted recessed gated devices (Figure 3c) no sign of newly generated traps on the AlGaIn surface can be seen. The absence of a decrease in slope and consequent shift in knee voltage as well as the increase in I_{dmax} (more pronounced than for slanted gated devices) indicates that stress has induced barrier traps underneath the gate which dominate the degradation (Figure 5b). Figure 3 therefore shows different locations for stress-induced trap generation: predominant signs for surface trapping in I-shaped gated devices and predominant signs of barrier trapping underneath the gate for slanted recessed gated devices. Slant non-recessed devices showed no significant degradation, i.e. only small amounts of trap generation.

Gate leakage measurements on the different HEMT gates are shown in Figure 5a. Devices with I-shaped gates exhibit a higher gate leakage current, while devices with the slant gate show almost an order of magnitude lower gate leakage. Gate leakage currents for devices with slant recessed gates are in the range of -2×10^{-6} to -4×10^{-6} mA/mm, i.e. about 6 orders of magnitude lower than for HEMTs with an I-shaped gate. For the I-shaped gated device the gate leakage current increased notably with stress while this was not observed for the devices with slant and slant recessed gates.

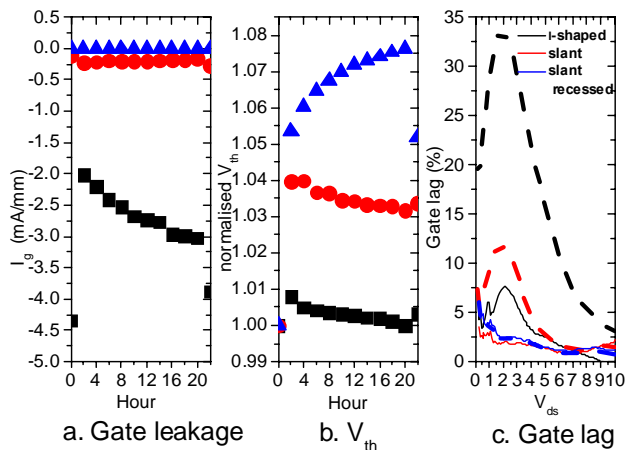


Figure 5 (a) Gate leakage currents, (b) normalized threshold voltage during device stress, (c) gate lag before and after stress for I-shaped (squares), slant (circles) and slant recessed gates (triangles). Percentages for gate lag refer to the ratio of the difference between DC and pulsed measurements to DC values for varying drain source voltage. Solid lines display before stress measurements while dashed represents after stress measurements.

There were only small changes of gate leakage current for the slant gated device induced by stress, while no significant change of leakage current was seen for the slant recessed gated device. Results of gate lag measurements, where the device was pulsed from a quiescent point of pinch off to open channel, are displayed in Figure 5c. The maximum gate lag increased from $\sim 8\%$ to almost 34% after stressing for the I-shaped gated devices while the slant gated devices show a gate lag of about 2-3% before stress and 12% afterwards. The slant recessed gated devices show a gate lag similar to that of the slant gated devices before stress, which did not change with stressing, however. Gate lag induced by the presence of traps is dependent on the electric field strength on the surface of the device [2], i.e. at the $\text{SiN}_x/\text{AlGaIn}$ interface. Differences in gate lag level between devices with different gate shapes that are observed prior to stress therefore illustrate not only differences in the number of active traps, but are also related to differences in electric field at the $\text{SiN}_x/\text{AlGaIn}$ interface at the gate corner produced by the different gate shapes. Note that the devices tested here were fabricated on the same wafer, the only difference between devices being in fact their gate shape. An increase in gate lag with stress obviously shows an increase in active traps on the surface that have been generated by the electric field. Following from this, it can be concluded that stress in the I-shaped gate strongly results in surface trap generation. Slant gated devices on the other hand have a smaller contribution from surface traps and slant recessed gates show basically no gate lag at all, i.e. no significant numbers of traps are contributing to the operation of the devices investigated here. These results are consistent with those from the DC output characteristics of Figure 3, which also showed dominant surface trapping for I-shaped gates and indications of barrier trapping for slant and slant recessed gates.

Figure 6 shows the result of I_d transient measurements before stress, after stress and after a day of device inactivity. Trapping characteristics illustrate the trap time constants through peak position along the x-axis and density of traps present and active in the devices through peak height. The traps observed here are denoted in the following as Tp1, Tp3 and Tp3' using the same convention as in Ref [4, 20] where measurements showed a dominant Tp1 peak that evolved into a more complex defect with different activation energies with stress while no further conclusions were drawn about trap levels Tp2 and Tp3 whose peak trap density (i.e. peak height) also increased with stress. We note that Tp2 as observed in Ref [4, 20] is not clearly apparent in the measured data here. The interpretation of the I_d transient measurement technique used here, is based on the reasonable assumption that any occupied electron trap in the AlGaIn layer or buffer underneath the gate will be emptied by the filling pulse in the measurement due to electrostatics, whereas surface electron traps in the access region

will be filled by electron capture assisted by leakage current from the gate [21, 22]. Hence the sign of the derivative of the transient gives a convincing indication of trap location with positive values indicating electron emission from surface traps and negative values indicating electron capture from the channel [22]. In the case studied here, Tp1 and Tp3 are therefore proposed to be surface traps, while Tp3' is proposed to be a barrier or bulk trap. As all measurements are performed after UV illumination, including the control measurement after 8hrs of device inactivity, any increase or decrease of the peak amplitude of Tp1, Tp3 and Tp3' represents the generation of such surface or bulk/barrier traps. We also note the difference in the I_d transient signal between the unstressed devices with different gate shapes. Both slanted gated devices, non-recessed and recessed, show a much lower peak amplitude and even the appearance of a barrier/bulk trap (Tp3') while I-shaped gated devices have high positive peak amplitudes. As all devices were fabricated on the same wafer these differences in the trapping spectra are related to carriers being injected and collected via the gate into and from traps present and activated without stressing. Different strength and peak electric field position and location of the gate with respect to the different device layers will affect how effectively different traps can be observed.

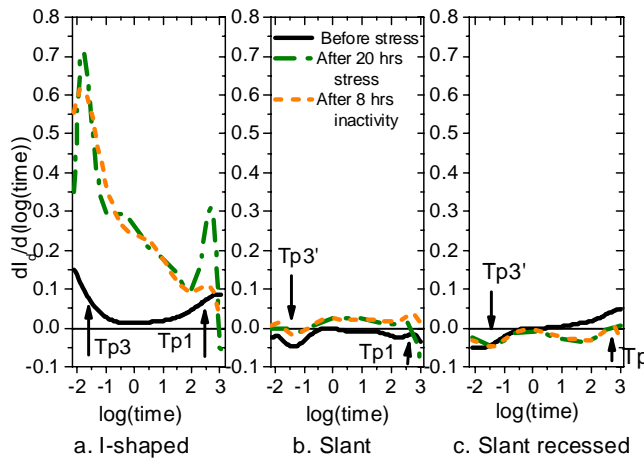


Figure 6 Comparison of derivatives of transient measurements for (a) I-shaped, (b) slant and (c) slant recessed gate shapes: Before stress (solid black line), after 20 hrs off-state stress at $V_{ds}=20V$ (dash-dot green line), 8 hrs device inactivity (dashed orange line). All measurements taken after UV illumination.

For I-shaped and slant gate devices, Figure 6 shows an increase of the trapping characteristics which had originally positive amplitudes, i.e. only contributions from surface traps. This increase was much stronger for I-shaped gated HEMTs and therefore consistent with the previous conclusions of stronger degradation for this type of gate shape through generation of surface traps. Slant non-recessed gated devices show a similar development as I-shaped gated devices in the sense that peak amplitudes become

slightly more positive. This could suggest the presence of a small surface trapping effect. In contrast, devices with a slant recessed gate, which exhibit a bulk trap Tp3' (negative signal) and surface trap Tp1 (positive signal) prior to stress show a stress induced shift into negative peak amplitudes for slower traps indicating increased trapping in the barrier or buffer underneath the gate. The existence of barrier or buffer traps underneath the gate may not be surprising given the possibility of etch-induced damage in the AlGaN during the gate recessing.

These different trap generation locations for the different gate shapes are consistent with a series of I_d transient measurements performed one after the other at different gate filling pulse voltages, as illustrated in Figure 7. No electrical stress was performed during this measurement. As the initial gate filling pulse fills surface traps next to the gate and empties barrier and buffer traps underneath the gate, the signal from both surface traps and buffer traps, i.e. electron emission and capture during data collection, is expected to decrease with decreasing filling pulse voltage magnitude.

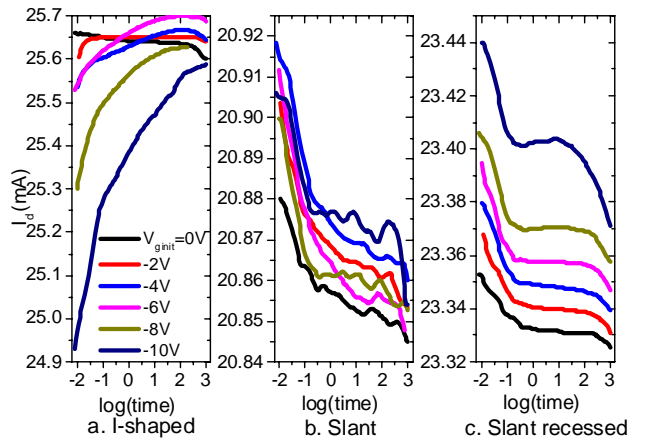


Figure 7 Transient measurements (showing the total drain current rather than the derivative) without UV illumination for (a) I-shaped, (b) slant and (c) slant recessed gates performed at different initial gate voltage pulses measured immediately after one another starting with a -10V pulse and reducing it by 2V for each measurement. Note different y-axis scales.

However, the effect of filling pulse magnitude on bulk traps in the barrier underneath the gate is expected to be less pronounced as this region is completely depleted when applying a filling pulse $\leq V_{th}$ as discussed in Ref [19]. In Figure 7 it is apparent that for the I-shaped gated devices there is an increase in I_d measured with decreasing filling pulse magnitude. This is consistent with the picture of surface traps being generated in this device by the device stress. For both slant gate variants I_d decreases with time for all filling pulse amplitudes consistent with electron capture predominantly by bulk traps underneath the gate.

As the passivation layer is deposited first for the slant gated devices, so that an etching process is involved in the fabrication of these devices, while it is not for the fabrication of I-shaped gated devices, trapping effects due to process induced damage are likely to influence the device. This can be seen in the presence of a bulk trap $Tp3'$ prior to stress for slant gated devices while I-shaped gates show the presence of a surface trap $Tp3$.

A difference in peak electric field for different gate shapes has been reported previously through measurement and simulation [23, 24]. In order to gain a physical understanding of the basis of the different degradation mechanisms observed between different gate shapes, electric field distributions for the same gate geometries and dimensions as those used in the experiments were simulated using the Silvaco ATLAS software. The results are shown in Figure 8. It is confirmed that the electric field along the surface is indeed highest for the I-shaped gated devices while slant recessed gated devices produce the lowest electric field at the surface (Figure 8a). This supports experimental data which found high surface trap generation for I-shaped gates, reduced surface trapping for slant gates and no distinguishable surface trapping for slant recessed gates. These simulations are consistent with previously reported simulation results for gates with 90° and 45° sidewalls in GaN/AlGaIn/GaN HEMTs [25].

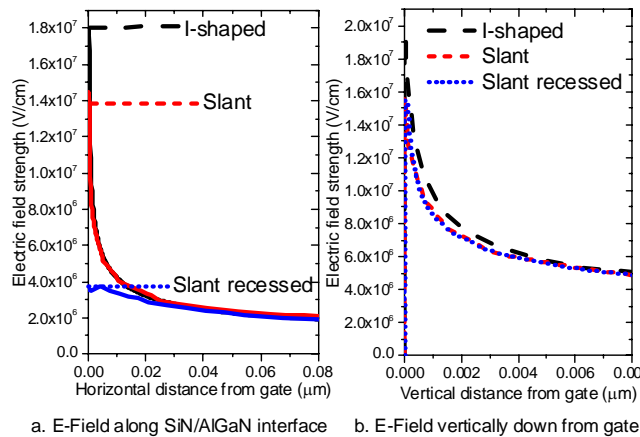


Figure 8 Simulation results of electric field magnitude (a) from the gate along the SiN_x/AlGaIn surface and (b) vertically down from the gate corner for I-shaped (black dashed line), slant (red short dashed line) and slant recessed (blue dotted line) gated devices at $V_{ds}=20V$ and $V_{gs}=V_{th}+0.5V$.

The corner of the I-shaped gate naturally enhances the electric field at the gate edges. This has the potential to cause the higher gate leakage current shown in figure 5a. Slanting the gate will result in reducing this electric field at the gate edge corner at the SiN_x/AlGaIn interface and is apparent in the reduction in gate leakage current, although this may also be associated with the CF₄ etch treatment

used for the slanted and slant recessed, but not the I-shaped gates. Moving the gate corner into the AlGaIn layer reduces the electric field at the SiN_x/AlGaIn interface even further; with the peak electric field now lying in the AlGaIn layer. Gate leakage mechanisms are suppressed for the recessed device as is shown experimentally in Figure 5a. Figure 8b shows electric field strength from the gate corner across the AlGaIn barrier to the channel. Note that the gate corner for the recessed devices is positioned 15nm into the AlGaIn barrier, so that the origin of the x-axis in Figure 8b corresponds to this position for the recessed devices, but corresponds to the SiN_x/AlGaIn interface for non-recessed devices. The electric field vertically down into the barrier is similar for all gate shapes. Experimental data suggests trap generation in the barrier underneath the gate for the slant recessed gate, which is likely due to etch damage in the AlGaIn layer.

4 Conclusions

AlGaIn/GaN HEMTs fabricated on the same wafer, i.e. using identical epitaxial material, but with different gate shapes, were investigated to assess the impact of the gate shape on degradation susceptibility. I-shaped gated devices not only showed sizable surface trapping prior to stress but also experienced the generation of surface traps during off-state stress. In contrast slant gated devices, with or without recess, showed little or no surface trap generation indicating the effectiveness of this approach to control the electric field at the gate corners. However, the slant gated devices, which require etching through the gate passivation before the gate deposition, showed trapping behavior consistent with traps located in the AlGaIn barrier before stressing most likely indicating some process induced damage within the bulk of AlGaIn. It is proposed that the off-state stress results in an increase in surface related trapping for the slant non-recessed gated devices, while increased barrier related trapping was identified for the slant recessed gated devices. Electric field strength at the gate corner and the SiN_x/AlGaIn interface is the driving force for trap generation in the degradation observed here. Simulation showed the peak electric field lay in the AlGaIn barrier for recessed devices but at the surface, i.e. the SiN_x/AlGaIn interface for non-recessed gates of both shapes.

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